Setting Standards in **VLSI** Design
Maven Silicon

Evolved in VLSI Technologies, Maven Silicon is a VLSI Training company that offers wide range of corporate and professional training services. Maven Silicon is the only training company in India that offers SystemVerilog and UVM based advanced verification courses and holds the credit of training 500+ engineers per year.

With shrinking process technologies, ever growing design sizes and increasing integration of IP to a single chip, verification has become extremely complex and critical part of any SoC design today. As the chip verification consumes 60% of the design cycle, most of the VLSI companies hire fresh VLSI engineers who have extensively been trained on ASIC verification methodologies and technologies and dedicate them only for chip verification. Usually 70% of the engineers in any product or services company dedicated only on functional verification and the remaining 30% of the engineers work on RTL design, STA and Analog etc. So there are plenty of job opportunities for fresh VLSI engineers who are highly skilled in ASIC verification. We at Maven Silicon have designed the courses keeping this fact in our mind. You can depend on our expertise and world class training infrastructure to learn the VLSI technologies and get a job in the top semiconductor industries.

Our CEO, Sivakumar P R has 20+ years of experience in engineering and semiconductor industries. He has worked as a Verification Consultant in the top EDA companies, Synopsys, Cadence and Mentor Graphics. During this tenure, he worked very closely with various ASIC and FPGA design houses and helped them to use the EDA solutions effectively, for the successful tape-outs of multi million gate designs.

To know more about our CEO, please visit http://www.linkedin.com/in/sivapr

FIVE REASONS TO MUSE

1. SystemVerilog and UVM based Advanced Verification
   Maven Silicon as the training centre edifies engineers on the advanced ASIC Verification methodologies and SystemVerilog. In addition to these advanced technologies, we also impart the basic VLSI technologies like Advanced Digital Design Methodology, Verilog, ASIC & FPGA’s design flow, STA & CMOS fundamentals.

2. Course Delivered by Industry Experts
   As courses such as VLSI-RN are composed of advanced VLSI design and verification technologies, only experienced VLSI engineers can deliver it. At Maven Silicon, industry experts share their experience and guide you on how to enhance your skills in VLSI Industries.

3. Superior Training Methodology
   At Maven Silicon, the experienced engineers who work in the top semiconductor industries share their experience with you and demonstrate how the concepts are applied in the real environment. Only 30% of 580 hours of VLSI-RN course is dedicated to impart concepts and remaining 70% for labs, mini projects and final project.

4. Excellent Placement Assistance
   Our CEO, Sivakumar is the Founder and CEO of a VLSI design services company called Aceic Design Technologies. We recruit the top performers of Maven Silicon for our services company and provide them great opportunities to work on complex verification projects, with industry best salary package.To know more about our services company, please visit www.aceic.com

   We work closely with various VLSI product and services companies and identify the right opportunities for the students who successfully complete our training program. Most of the students have been successfully placed in renowned semiconductor companies.

5. Excellent work environment
   We provide excellent work environment, which has adequate hardware and software infrastructure. Maven Silicon has chosen Mentor Graphics as its EDA partner and provides great opportunities to engineers to work on verification platform like Questa and explore the advanced ASIC verification technologies and methodologies.

EDA Partner - Mentor Graphics

Mentor Graphics is leader in Electronic Design Automation. Its innovative products and solutions help engineers conquer design challenges in seemingly daunting world of board and chip design.

To know more about Mentor Graphics, please visit www.mentor.com

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MODULE 1
Introduction to VLSI
- VLSI Design Flow
- ASIC Vs FPGA
- RTL Design Methodologies
- Introduction to ASIC verification methodologies

VLSI Design Flow Steps – Demo

MODULE 2
Introduction to Linux
- Components of UNIX system
- Directory Structure
- Utilities and Commands
- Vi Editor

MODULE 3
Advanced Digital Design
- Introduction to Digital Electronics
- Arithmetic Circuits
- Data processing Circuits
- Universal Logic Elements
- Combinational Circuits - Design and Analysis
- Latches and Flip flops
- Shift Registers and Counters
- Sequential Circuits - Design and Analysis
- Memories and PLD
- Finite State Machine
- Microcontroller Design

MODULE 4
Static Timing Analysis
- Introduction to STA
- Comparison with DTA
- Timing Path and Constraints
- Different types of clocks
- Clock domain and Variations
- Clock Distribution Networks
- How to fix timing failure

MODULE 5
CMOS Fundamentals
- Non Ideal characteristics
- BJT vs FET
- CMOS Characteristics
- CMOS circuit design
- Transistor sizing
- Layout and Stick Diagrams
- CMOS Processing Steps
- Fabrication
- CMOS Technology- Current Trends

MODULE 6
Verilog HDL – RTL Coding and Synthesis
[1] Introduction to Verilog HDL
- Applications of Verilog HDL
- Verilog HDL language concepts
- Verilog language basics and constructs
- Abstraction levels

[2] Data Types
- Type concept
- Nets and registers
- Non hardware equivalent variables
- Arrays

[3] Verilog Operators
- Logical operators
- Bitwise and Reduction operators
- Concatenation and conditional
- Relational and arithmetic
- Shift and Equality operators
- Operators precedence

[4] Assignments
- Types of assignments
- Continuous assignments
- Timing references
- Procedures
- Blocking and Non-Blocking assignments
- Execution branching
- Tasks and Functions

- Basic FSM structure
- Moore Vs Mealy
- Common FSM coding styles
- Registered outputs

- System Tasks
- Internal variable monitoring
- Compiler directives
- File input and output

[7] Synthesis Coding Style
- Registers in Verilog
- Unwanted latches
- Operator synthesis
- RTL Coding Style

MODULE 7
Code Coverage
- Statement coverage
- Branch Coverage
- Expression Coverage
- Path Coverage
- Toggle Coverage
- FSM - State, Arc and Sequence coverage

MODULE 8
FPGA Architecture
[1] PLD
- General Structure and Classification
- CPLD Vs FPGA

[2] Xilinx CPLD - Xc9500
- Block Diagram of CPLD
- Detailed study of each block
- Endurance limits
- Timing Model

[3] Xilinx FPGA
- FPGA Architecture
- CLBs and Input/Output Blocks
- LUTs, SLICE DFFs
- Dedicated MUXes
- Programmable Interconnects
- Architectural Resources
- Power Distribution and Configuration


MODULE 9
Verilog Mini Project
- RTL Coding and Synthesis
  - Project Specification Analysis
  - Understanding the architecture
  - Module level implementation and verification
  - Building the top level module
  - Implementing the design onto the FPGA board

MODULE 10
Design Automation using Scripts
- Perl
  - Introduction to Perl
  - Functions and Statements
  - Numbers, Strings, and Quotes
  - Variables
  - Comments and Loops

MODULE 11
Soft Skill Workshop
- Communication Skills
- Mock up Interview
- Group Discussion
- Behavioural traits
- Interpersonal skills
- Time and Project Management

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### MODULE 12
**ASIC Verification Methodologies**
- Directed Vs Random
- Functional verification process
- Stimulus Generation
- Bus function model
- Monitors and reference models
- Coverage Driven Verification
- Verification Planning and management

### MODULE 13
**SystemVerilog HVL**

1. **[1] Introduction to SystemVerilog**
   - New Data types
   - Tasks and Functions
   - Interfaces
   - Clocking blocks

2. **[2] Object Oriented Programming and Randomization**
   - OOP Basics
   - Classes – Objects and handles
   - Polymorphism and Inheritance
   - Randomization
   - Constraints

3. **[3] Threads and Virtual Interfaces**
   - Fork Join
   - Fork Join_any
   - Fork Join_none
   - Event controls
   - Mailboxes and semaphores
   - Virtual Interfaces
   - Transactors
   - Building verification environment
   - Testcases

4. **[4] Callbacks**
   - Facade Class
   - Building Reusable Transactors
   - Inserting Callbacks
   - Registering Callbacks

5. **[5] Direct Programming Interface**

   - Coverage models
   - Coverpoints and bins
   - Cross coverage
   - Regression testing

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### MODULE 14
**Verification Planning and Management**
- Verification Plan
- TB Architecture
- Coverage Model
- Tracking the simulation process
- Building regression testsuite
- Testsuite optimization

### MODULE 15
**Advanced SystemVerilog**
- Environment Configuration
- Reference Models and Predictor Logics
- Using Legacy BFM
- Scenario Generation
- Testcases - Random, Directed and corner case
- Coding styles for VIP

### MODULE 16
**Assertion Based Verification – SVA**
- Introduction to ABV
- Immediate Assertions
- Simple Assertions
- Sequences
- Sequence Composition
- Advanced SVA Features
- Assertion Coverage

### MODULE 17
**Verification Mini Project: Verification and RTL sign-off**
- Project specification analysis
- Defining verification plan
- Creating Testbench architecture
- Defining Transaction
- Implementing the transactors - Generator, Driver, Receiver and Scoreboard
- Implementing the coverage model
- Building the top level verification environment
- Defining weighted random, corner case and directed testcases
- Building the regression testsuite
- Generating the functional and code coverage reports

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### EDA TOOLS
- Mentor Graphics
- Xilinx
- Aldec

### OPERATING SYSTEM
- Linux - Ubuntu